Cable Compensation of a Primary-Side-Regulation (PSR) Power Supply

Abstract

Cable compensation has been used to compensate the voltage drop due to cable impedance for providing a regulated charging voltage in battery charger applications. This application note uses a novel cable compensation method, which called cable minus compensation, as an example to describe the concept and design criteria for the cable compensation of a primary-side-regulation (PSR) flyback converter. The analytic results are also verified by the simulation results.

1. Introduction

A flyback converter with primary-side-regulation (PSR) is widely used in off-line battery charger applications due to low cost and simplicity. In a PSR, the output voltage is indirectly sensed through the auxiliary winding, and good regulation can be achieved with the precise detection circuit. However, in such applications, there is a long cable connected between the adaptor output and the electronic devices, such as cell phone, tablet, and so on. If the output voltage is perfectly regulated, there is a voltage drop at the cable end while the output current flows through the cable impedance. The decreasing charging voltage will extend the charging time and even violate the regulation specification especially for the situation under low output voltage and high output current application. This phenomenon can be illustrated in Figure 1.

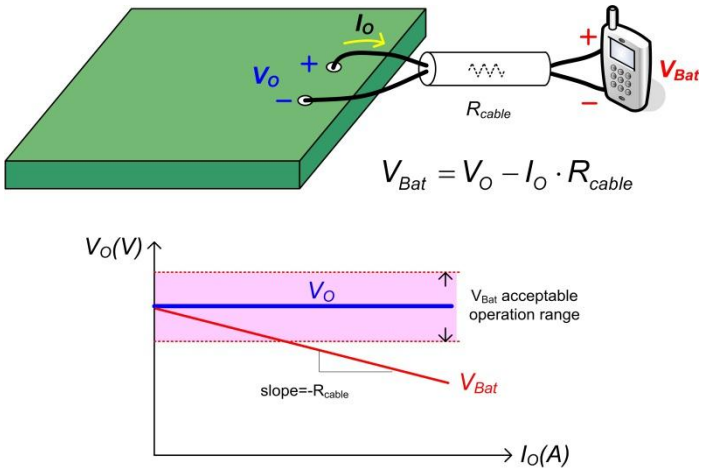

Figure 1. The Voltage Drop Due to Cable Impedance

Cable compensation is used to compensate the cable voltage drop by linearly increasing the output voltage V_O with the output current I_O. Figure 2 shows these two methods used to realize cable compensation. One is called cable plus compensation, which adds the compensation signal $K \cdot I_O$ to the reference voltage V_{REF} and feeds into the non-inverting terminal of the error amplifier. The desired compensation voltage can be accurately reflected on the increment of the reference voltage through the compensation signal $K \cdot I_O$, and the DC gain K can be obtained from (1). The other is called cable minus compensation. This scheme subtracts the compensation signal $K \cdot I_O$ from the feedback voltage V_{FB} and pass through Z_i into the inverting terminal of the error amplifier.

$$\frac{V_{REF}}{V_{REF}+K\cdot I_O}=\frac{V_{Bat}}{V_{Bat}+I_O\cdot R_{cable}} \quad (1)$$

However, the output current cannot directly be sensed in PSR applications. Figure 3 shows the circuit diagram of a PSR flyback converter with cable minus compensation. In the diagram, the compensation signal is injected from the signal V_{CS} in the primary side through a buffer with compensator DC gain K_{CC} and a low pass filter (LPF) to indirectly estimate the output current. Current sensing resistor R_S is used to transfer the voltage signal V_{CS} from the primary side current signal I_P. If the cutoff frequency of LPF or the DC gain K_{CC} is not properly designed, the output voltage may incur oscillation problem and the circuit will be unstable. Therefore, a comprehensive small signal analysis will be provided in the following section for the cable compensator and the feedback control design of a PSR flyback converter.

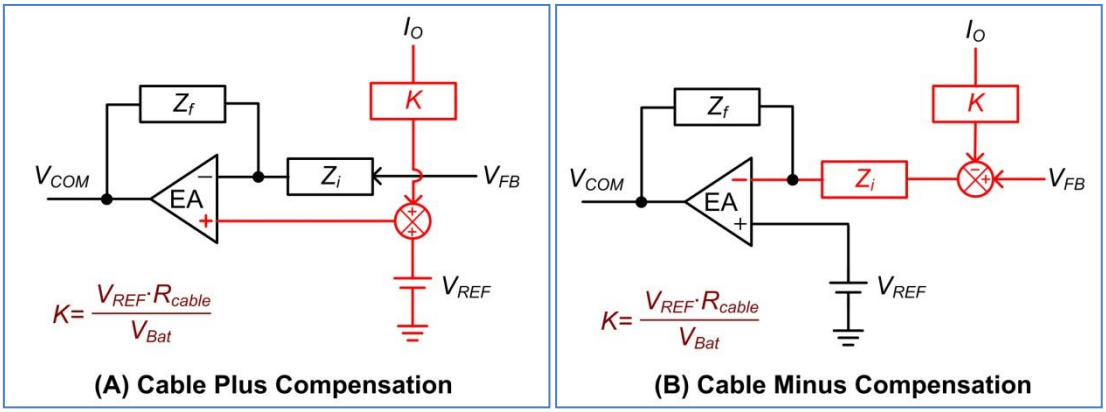

Figure 2. Cable Compensation Implementation Methods with (A) Cable Plus Compensation, and (B) Cable Minus Compensation.

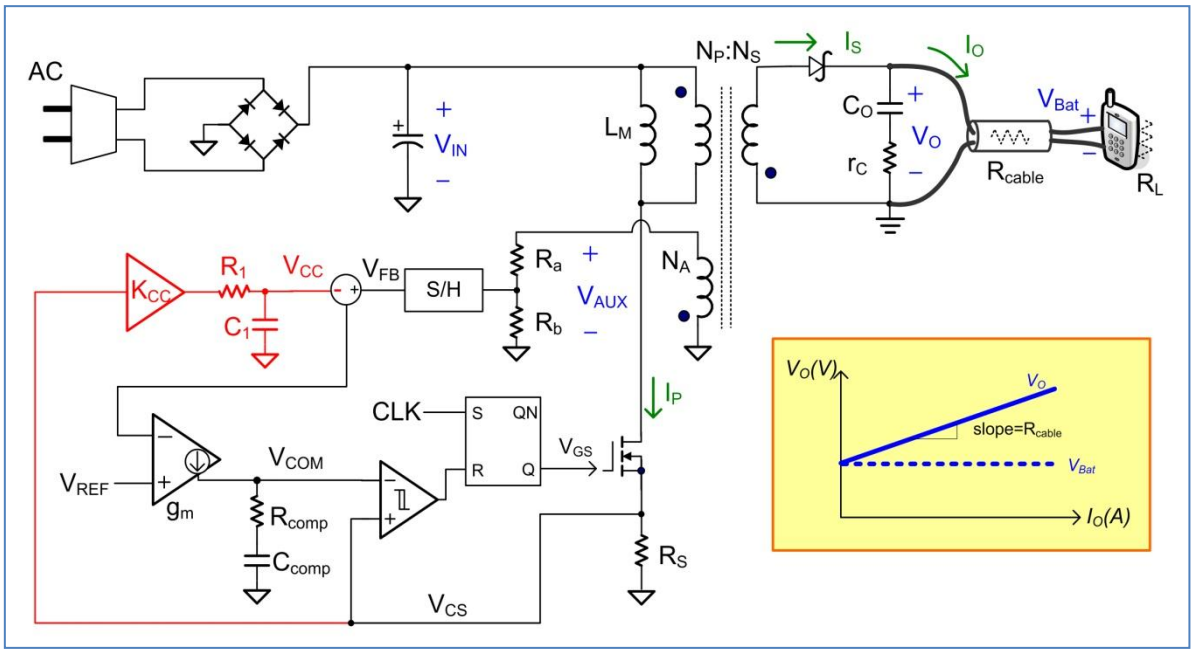

Figure 3. Circuit Diagram of a PSR Flyback Converter with Cable Minus Compensation.

2. Small Signal Analysis of a DCM PSR Flyback Converter with Cable Compensation

Figure 4 shows the control block diagram of a DCM PSR flyback converter with cable minus compensation. Table I summaries the transfer functions used in the control block diagram. From the control block diagram as shown in Figure 4, there are two loop gains T_1 and T_2, which are respectively measured at point A and point B, can be found in the feedback loop. They can be expressed as (2) and (3) with reference to the voltage loop gain T_V and the current loop gain T_C. T_V and T_C can be respectively represented as (4) and (5).

$$T_1(s) = T_V(s) - T_C(s) \quad (2)$$

$$T_2(s) = \frac{T_V(s)}{1 - T_C(s)} \quad (3)$$

$$T_V(s) = G_{EA}(s) \cdot F_m \cdot G_{do}(s) \cdot K_D \cdot G_{SH}(s) \quad (4)$$

$$T_C(s) = G_{EA}(s) \cdot F_m \cdot K_{DP} \cdot R_s \cdot G_{cc}(s) \quad (5)$$

When the cable compensation involves in the feedback loop, it is surprisingly found that the loop gain T_2 is a positive feedback loop which the output voltage V_O has the same phase with the error amplifier output V_{COM}. The positive feedback loop tends to let system become unstable. However, the system stability can be achieved by imposing a negative feedback loop. The loop gain T_1 provides a negative feedback loop and is used to determine the system stability. The stability criterion needs to be fulfilled by letting the loop gain T_1 cross 0 dB with –20 dB/decade slope and have adequate phase margin.

Although the loop gain T_2 is not used to determine the system stability, it influences the output impedance. From the control block diagram shown in Figure 4, the output impedance can be obtained as (6). Not like the traditional thinking, the output impedance is designed to be as low as possible for achieving good load regulation. In order to provide proper cable compensation, the output impedance is expected to have a negative impedance to mitigate the cable impedance. If the output impedance can be designed as $-R_{cable}$, the cable impedance seems to be cancelled and the charging voltage is regulated without voltage drop.

$$Z_{O\_closed}(s) = \frac{Z_O(s)}{1 + T_2(s)} \quad (6)$$

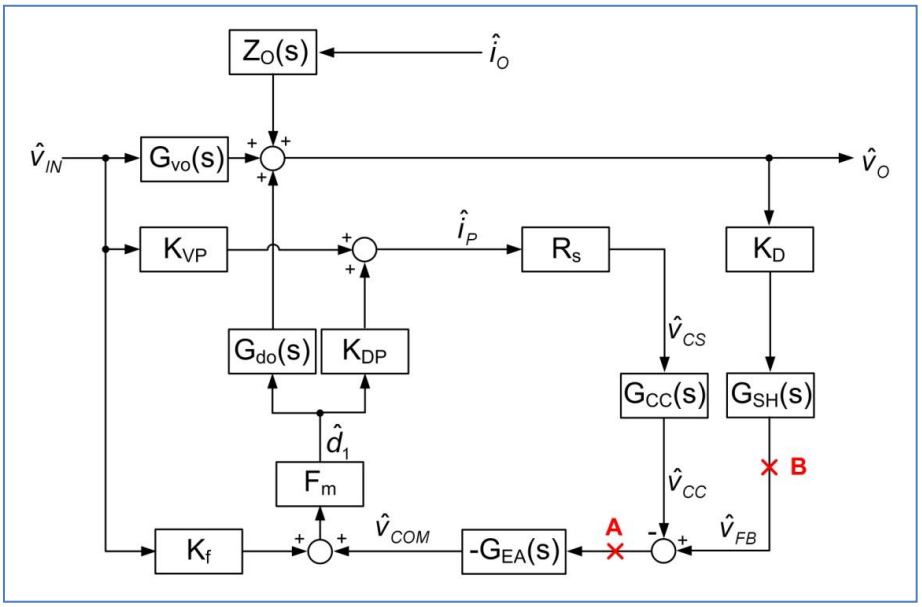

Figure 4. Control Block Diagram of a DCM PSR Flyback Converter with Cable Minus Compensation.

Table I : Transfer Functions of a DCM PSR Flyback with Cable Compensation.

Control to output	$G_{do}(s)=\frac{V_o}{D_1}\cdot\frac{1+s\cdot C_o\cdot r_c}{1+s\cdot\frac{C_o\cdot R_L}{2}}$
Line to output	$G_{vo}(s)=\frac{V_o\cdot N_p}{V_{IN}\cdot N_s}\cdot\frac{1+s\cdot C_o\cdot r_c}{1+s\cdot\frac{C_o\cdot R_L}{2}}$
Open loop output impedance	$Z_o(s)=\frac{R_L}{2}\cdot\frac{1+s\cdot C_o\cdot r_c}{1+s\cdot\frac{C_o\cdot R_L}{2}}$
Voltage divider gain	$K_o=\frac{N_A}{N_s}\cdot\frac{R_b}{R_a+R_b}$
Compensator	$G_{EA}(s)=\frac{g_m}{C_{comp}}\cdot\frac{1+s\cdot R_{comp}.C_{comp}}{s}$
Cable compensator	$G_{cc}(s)=\frac{K_{cc}}{1+s\cdot R_1\cdot C_1}$
Modulation gain	$F_m=\frac{L_M}{V_{IN}\cdot R_s\cdot T_s}$
Feed forward gain	$K_f=\frac{-D_1\cdot R_s\cdot T_s}{L_M}$
Sample & hold	$G_{SH}(s)=\frac{1-e^{-T_s}}{s\cdot T_s}$
Line to primary side current gain	$K_{vp}=\frac{D_1^2\cdot T_s}{2\cdot L_M}$
Duty to primary side current gain	$K_{DP}=\frac{V_{IN}\cdot D_1\cdot T_s}{L_M}$

3. Feedback Control Design

Cable compensation can be effectively accomplished by subtracting the compensation signal $K \cdot I_O$ from the feedback voltage V_{FB}. However, in PSR applications, the average signal of V_{CS} with a DC gain K_{CC} is fed as the compensation signal instead. In order to achieve proper cable compensation, the DC gain K_{CC} can be obtained from (7). Lower K_{CC} leads to the output voltage under-compensated, but higher K_{CC} causes the output voltage over-compensated and may incur unstable problem.

$$K_{CC} = \frac{I_O}{I_{IN} \cdot R_S} \cdot K = \frac{V_{IN} \cdot V_{REF} \cdot R_{cable}}{V_{Bat}{}^2 \cdot R_S} \quad (7)$$

LPF is used to obtain the average value of $K_{CC} \cdot V_{CS}$ by filtering out the high switching frequency part. When the cutoff frequency is lower, the high frequency signal of $K_{CC} \cdot V_{CS}$ can be effectively attenuated and the system tends to be more stable. However, it will pay more area with larger passive components and become unattractive for the practical integrated circuit design. Therefore, the cutoff frequency is a trade-off design between the component size and the system performance.

The goal of the compensator design is to find proper compensator gain G_{EA} such that the loop gain T_1 can meet the bandwidth requirement with specified phase margin. The compensator can be designed according to (8) and (9). When the magnitude of $G_{do} \cdot K_D$ is larger than $K_{DP} \cdot R_S \cdot G_{CC}$, G_d can be approximated to $G_{do} \cdot K_D$, which has one pole and one zero at the left hand plane. The compensator can be easily designed like traditional voltage mode control without considering the current loop T_C. It provides one pole at origin and one compensation zero to cancel the system's pole to make the loop gain T_1 stable by crossing 0 dB with –20 dB/decade slope.

However, when the magnitude of $K_{DP} \cdot R_S \cdot G_{CC}$ approaches $G_{do} \cdot K_D$, there are two poles and two zeros existing in G_d as shown in (9). As the cutoff frequency of LPF gradually increases, the magnitude of $K_{DP} \cdot R_S \cdot G_{CC}$ starts to be larger than $G_{do} \cdot K_D$ during some frequency range as shown in figure 5. When this situation happens, the two left-half-plane zeros of G_d move to the right-half-plane and the system tends to become unstable. Therefore, the compensator can be designed from (8) by neglecting $K_{DP} \cdot R_S \cdot G_{CC}$ first. The cutoff frequency of LPF can then be design to let $K_{DP} \cdot R_S \cdot G_{CC}$ be always less than $G_{do} \cdot K_D$ for system stability.

$$T_1(s) \approx G_{EA}(s) \cdot F_m \cdot \left[G_{do}(s) \cdot K_D - K_{DP} \cdot R_S \cdot G_{cc}(s) \right] = G_{EA}(s) \cdot F_m \cdot G_d(s) \quad (8)$$

$$G_d(s) = \frac{\frac{K_D \cdot Vo}{D_1} \cdot \left(1 + s \cdot C_o \cdot r_c\right) \cdot \left(1 + s \cdot C_1 \cdot R_1\right) - K_{DP} \cdot R_S \cdot K_{cc} \cdot \left(1 + s \cdot \frac{C_o \cdot R_L}{2}\right)}{\left(1 + s \cdot \frac{C_o \cdot R_L}{2}\right) \cdot \left(1 + s \cdot C_1 \cdot R_1\right)} \quad (9)$$

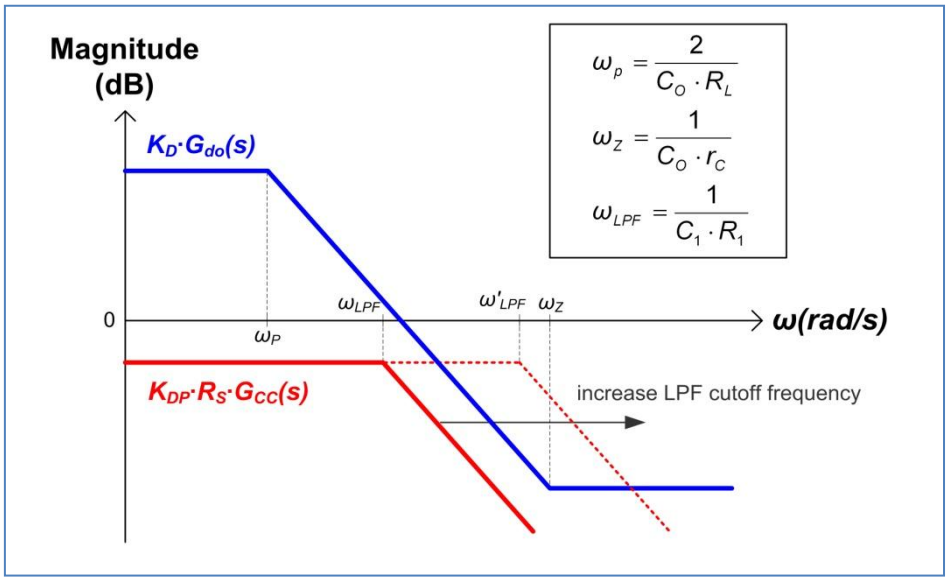

Figure 5. The Plots of $K_{DP} \cdot R_S \cdot G_{CC}$ and $G_{do} \cdot K_D$.

4. Simulation Verification

Simulation is used to verify the analytic results, and the parameters are listed as follows. V_{IN} = 156V, V_{Bat} = 5V, I_O = 1A, L_M = 1.5mH, C_O = 1mF, r_C = 20mΩ, R_S = 4.5Ω, R_{cable} = 240mΩ, N_P : N_S : N_A = 15:1:1.4, f_S = 50kHz, V_{REF} = 1.2V, g_m = 100μA/V, R_{comp} = 215kΩ, C_{comp} = 12nF, R_a = 29kΩ, R_b = 6kΩ, R_1 = 100kΩ, C_1 = 5nF, and K_{CC} = 400m. Figure 6 shows the simulation waveforms with and without cable compensation, and cable compensation provides proper voltage drop compensation under different load conditions. Figure 7 and figure 8 respectively show the loop gains T_1 and T_2. The simulation results are well matched with the calculation results. The system bandwidth and phase margin can be determined form the loop gain T_1, and it can be observed that the loop gain T_2 is a positive feedback. Figure 9 shows the output impedance. The DC gain of the output impedance is close to R_{cable} but the phase starts from 180°, which means it can provide negative impedance for effectively cancelling the cable impedance.

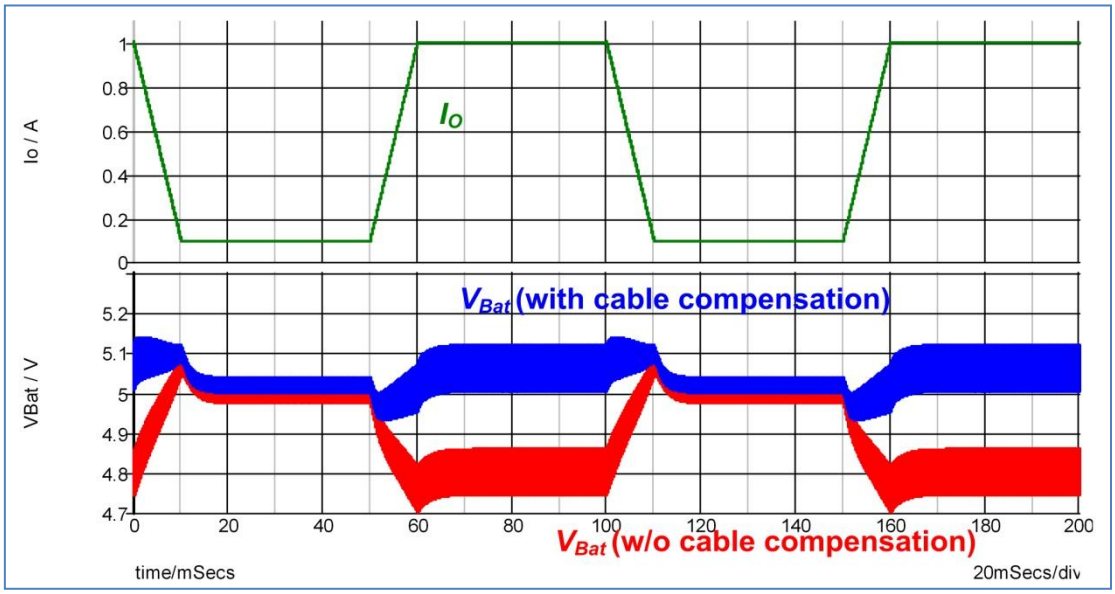

Figure 6. Simulation Waveforms with and without Cable Compensation.

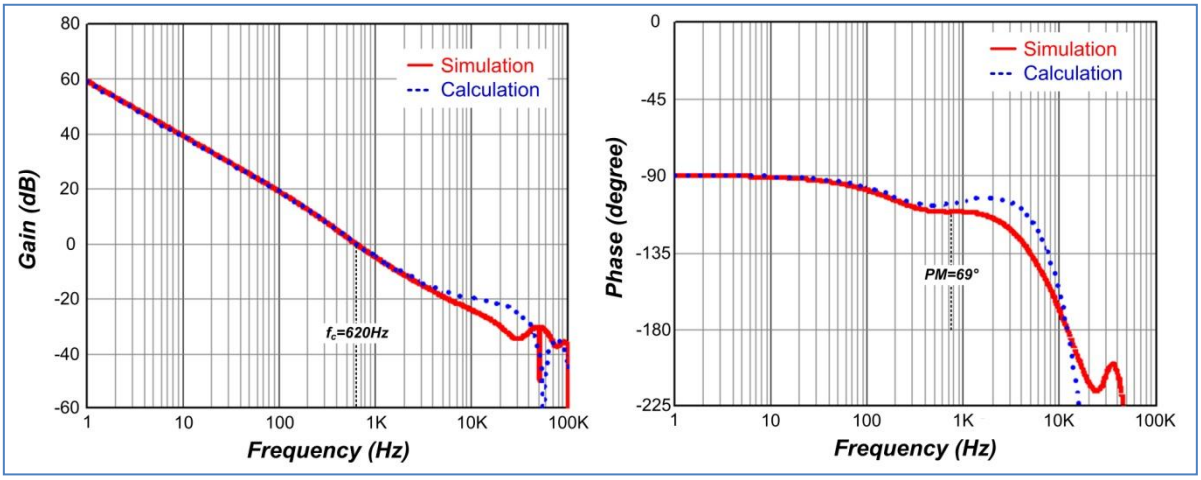

Figure 7. Bode Plots of Loop Gain T_1

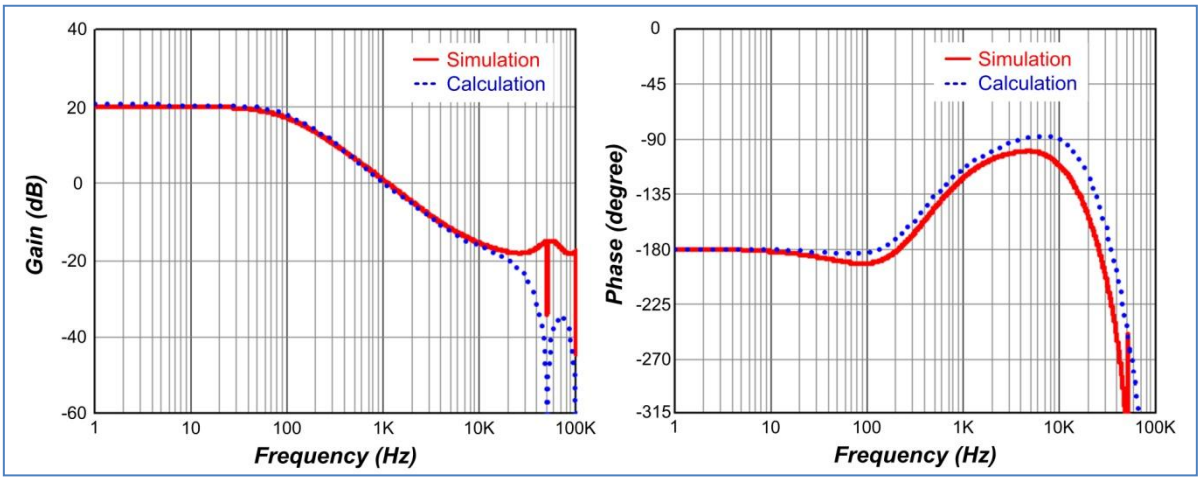

Figure 8. Bode Plots of Loop Gain T_2

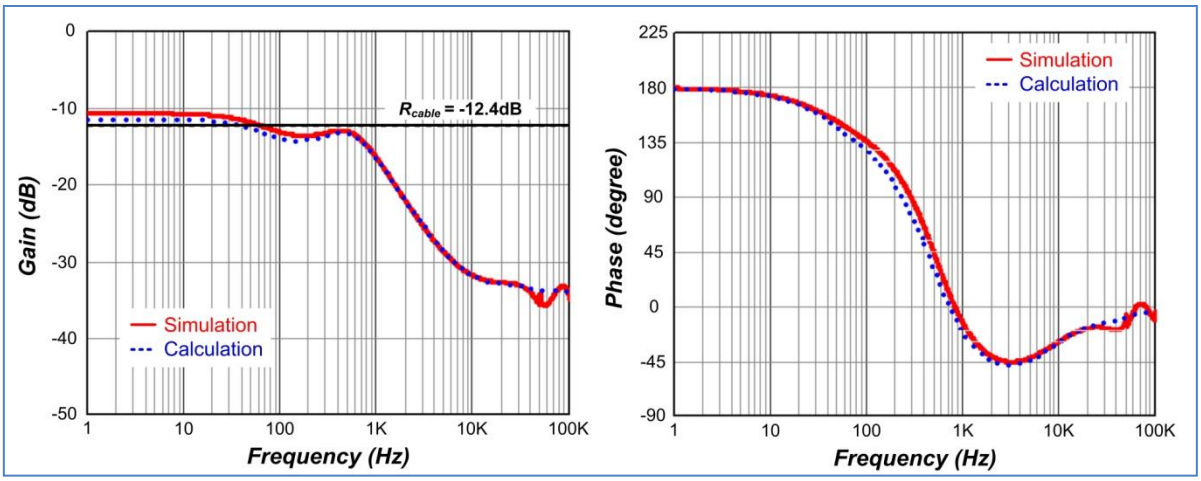

Figure 9. Bode Plots of the Output Impedance.

Figure 10 shows simulation and calculation results with different cutoff frequency of LPF by changing C_1. Higher cutoff frequency of LPF incurs unstable problem, and this instability phenomenon can also be predicted according to the loop gain T_1 proposed in the previous analytic result. The minimum value of C_1 can be determined from the plots of $K_{DP}{\cdot}R_S{\cdot}G_{CC}$ and $G_{do}{\cdot}K_D$ with fixed R_1. Figure 11 shows the plots of $K_{DP}{\cdot}R_S{\cdot}G_{CC}$ and $G_{do}{\cdot}K_D$ with different C_1 values, and it can be found C_1 has to be greater than 3nF for satisfying the condition that $K_{DP}{\cdot}R_S{\cdot}G_{CC}$ is always less than $G_{do}{\cdot}K_D$. The simulation also confirmed the result with the minimum C_1 equals to 4nF.

Figure 12 shows the bandwidth and the phase margin of loop gain T_1 with different C_1 values. From the figure, it can be found that the system tends to have higher bandwidth and phase margin with larger C_1 value. However, when C_1 is beyond certain value, the system performance has no significant improvement but extra component size is unnecessarily paid. Therefore, the small signal analysis proposed in this paper provides a useful tool to design the proper cutoff frequency of LPF.

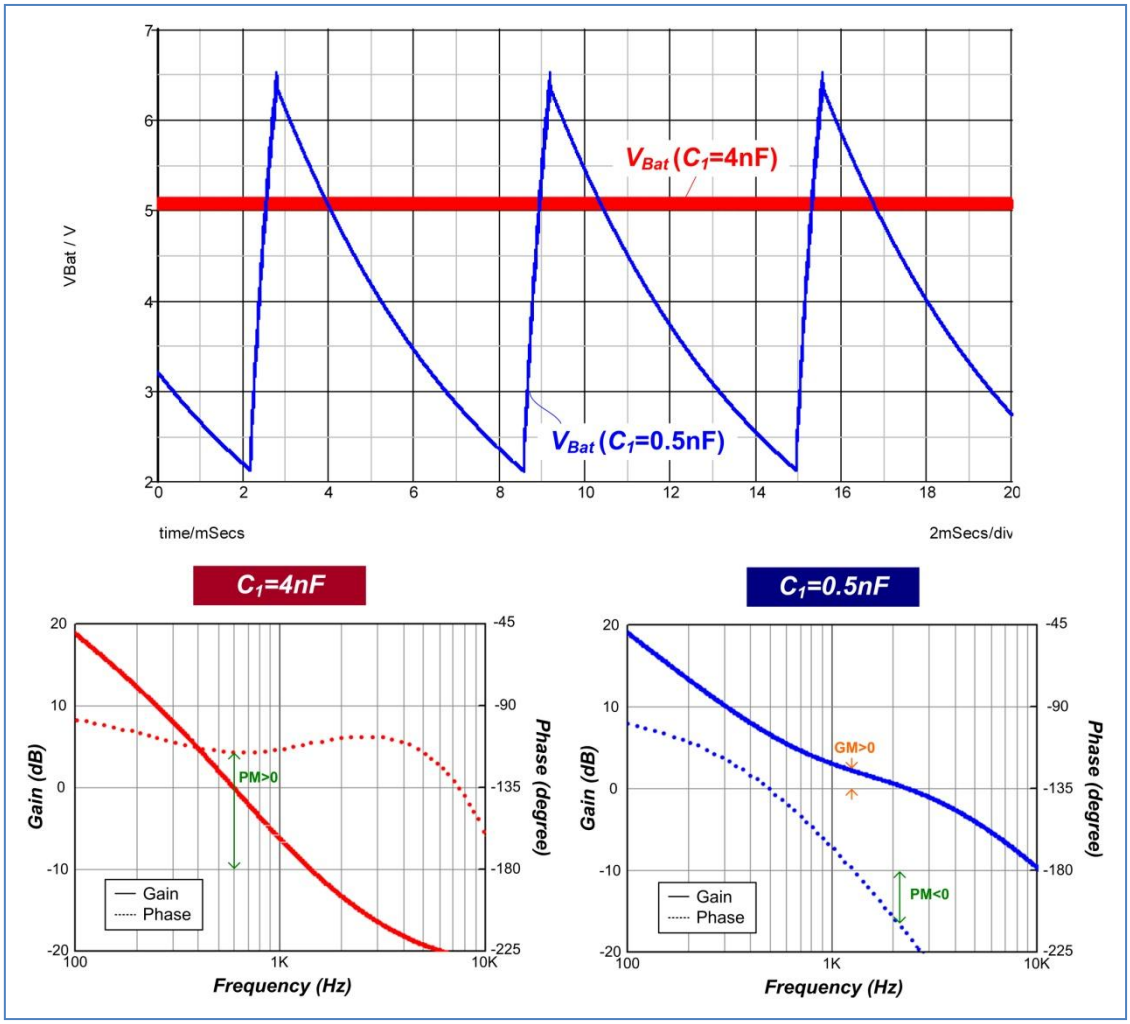

Figure 10. Simulation Waveforms of the Charging Voltage V_{Bat} and Calculation Results of Loop Gain T_1 with Different C_1

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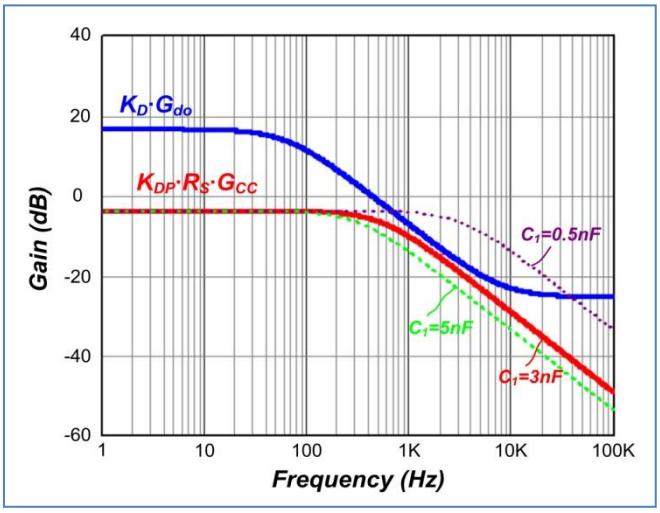

Figure 11. The Plots of K_{DP}·R_S·G_{CC} and G_{do}·K_D with Different C_1.

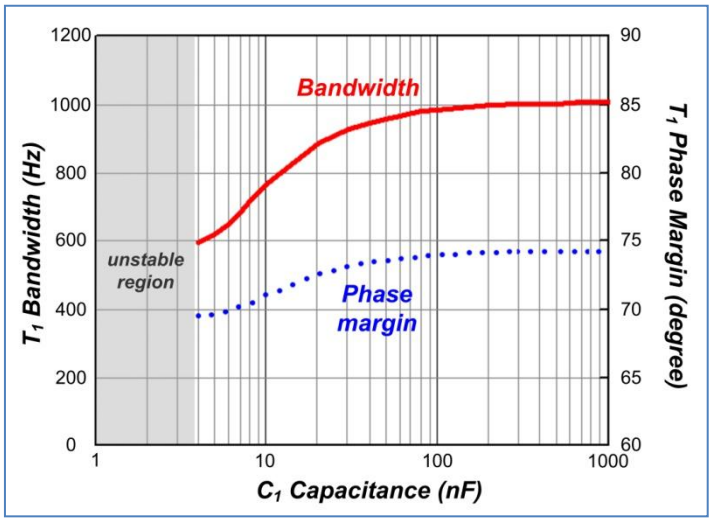

Figure 12. The Bandwidth and the Phase Margin of Loop Gain T_1 with Different C_1

5. Summary

A PSR flyabck converter with cable minus compensation was proposed to tackle the voltage drop due to the cable impedance in battery charger applications. The small signal model presented in this paper provided a comprehensive tool for small signal analysis and feedback control design to fulfill proper cable compensation. The analytic results were also explained and successfully verified by the simulation results.

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